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A REVIEW OF 2-10 GHZ LNA IN STANDARD CMOS USING DIFFERENT TOPOLOGIES

Barkha Chachwani*, Sanjana Verma, Saurabh Pargaien

* B.Tech, Electronics & Communication Department,Graphic Era Hill University Bhimtal,India
B.Tech, Electronics & Communication Department,Graphic Era Hill University Bhimtal,India
Assistant Professor,Electronics & Communication Department,Graphic Era Hill University Bhimtal,India

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ABSTRACT

LNA is the most important part of receiver system. For any LNA it is very essential to keep high gain with linearity and a low noise figure for its successive blocks in the system. This paper presents the literature review of various LNAs used for a frequency range from 2 GHz to 10 GHz. The most important parameters considered in a LNA are gain, noise figure, linearity and impedance matching. Current reuse, cascade amplifiers, cascoded amplifiers topology, source degeneration topology, resistive feedback, cross coupled capacitor technique, $g_{\_m}$-boosted current reuse topology, single stage, multistage are the defined techniques used for LNA design.

KEYWORDS: Low Noise Amplifier (LNA) , Noise Factor (NF) , Common Source Ultra wideband (CS-UWB) , Common Gate Ultra Wideband (CG-UWB).

INTRODUCTION

Power consumption, high gain, low noise, high linearity are the keyword of any communication system design. For any designer these parameters must be achieved for best performance. Small size, availability of multiple applications on a single system is in demand. RFIC designing is the key solution of this challenge. LNA's is an active research area and is of crucial importance for receiver in wireless technologies. A number of topologies and techniques are used for achi-eving the parameters of LNA. Common Source and the Common Gate LNA are two topologies that are used for designing any LNA. CS LNA output gate current noise increases with the incr-ease in frequency. In CGLNA noise factor is nearly constant irrespective of the frequency of operation and bandwidth.

STUDY OF EXISTING TECHNIQUES

The study of earlier work done by researchers/scientists is to considered before giving any final theories in this respective field. The earlier techniques and concepts given by researchers are very helpful for the analysis of the present high technology communication era. There is a growing demand of RFIC design to make device size small, portable and large frequency band applications. This paper presents brief review of the research done by various researchers in the area of the designing and simulating LNA's for frequency ranges from 2 GHz to 10 GHz.

W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. Pineda de Gyvez, D. J. Allstot, and E. Sanchez – Sinencio (2005) proposed a capacitor cross-coupled g_m-boosting scheme to reduce noise factor and current consumption. The achieved output gain was 7.1 dB, Noise figure of 3.0 dB at 6.0 GHz and power dissipation was 6.48 mW from a supply of 1.8 V. source. The measured input-referred third-order intercept (IIP3) value is 11.4 dBm [1].

Saman Asgaran, M. Jamal Deen, and Chih-Hung Chen (2006) proposed a fully integrated 5.7-GHz CMOS LNA. A simple L-C network is used in place of source degeneration to achieve 50 ohm parasitic impedance at input terminal. This method enhances the effective g_m of the LNA by a factor that is inversely proportional to a MOSFET's input

resistance. the proposed circuit has a power gain of 11.45dB with noise figure of 3.4-dB at 4 mW of dc power. The value of S_{11} is -14 dB and S_{22} -17 dB. [2]

Yi-Jing Lin, Shawn S. H. Hsu, Jun-De Jin, and C. Y. Chan (2007) proposed a ultra-wideband LNA using a current-reused technique. A simple high-pass LC network is used for input matching. Simulation results shows a power gain of 16 dB, noise figure of 3.1 – 6 dB in the frequency range of 3.1–10.6 GHz with the power dissipation of 11.9 mW in 1.8-V power supply.[3]

F. Gianesello, D. Gloria, C. Raynaud, S. Boret (2007) proposed the advantages of SOI CMOS over CMOS bulk. SOI can be preferred for reducing source/drain-substrate capacitance and elimination of body effect. It is suited for low voltage supply. LNA schematic is designed in 0.13 μm SOI CMOS technology using High Resistivity substrate. A NF of 1.4 dB at 5GHz and a gain of 14 dB with current of 8 mA under 1.2 V. [4]

Siu-Kei Tang, Kong-Pang Pun, Chiu-Sing Choy, Cheong-Fat Chan, and Ka Nang Leung (2008) proposed a band-selective LNA for multiband orthogonal frequency- division multiplexing ultra-wideband receivers which enhances the gain and noise performance of the LNA in each frequency band without increasing its power consumption. It achieves a gain of 16 dB, with a noise figure of 2.74 dB, and an third-order input intercept point of 8.8 dBm with a current consumption of 7.95 mA from a 1.5 V supply. [5]

Jouni Kaukovuori , Mikko Kaltiokallio and Jussi Ryynanen (2008) proposed a design of CG LNA for the wideband applications. The effect of the different components in matching network is analyzed in detail. The design of a wideband input matching and output signal current for the input stage and the effect of the matching network on the linearity and noise of a CG stage is studied. [6]

Jaewoo Park, Shin-Nyoung Kim, Yong-Seong Roh, and Changsik Yoo (2010) proposed a CMOS direct-conversion receiver by employing a voltage feedback in a common-gate low-noise amplifier (LNA). In the proposed schematic the input matching of the LNA can be reconfigured for each RF band by simply changing the resonant frequency of the load network. The frequency characteristics of the active-RC channel selection filter with an R-2R ladder is automatically tuned by a one-shot tuning circuit. The measured NF of the receiver implemented in a 0.18-μm CMOS process is 4.6–5.6 dB. [7]

Giuseppina Sapone, Member, IEEE, and Giuseppe Palmisano, Senior Member, IEEE (2011) proposed the design of a 90-nm CMOS LNA for 3–10 GHz ultra-wideband application by using a single-ended dual-stage solution. The first stage uses the current-reuse topology and performs UWB (3–10 GHz) input matching. The second stage is a cascode amplifier with resonant load which enhances the gain and reverse isolation. With these two stages the LNA provides input matching, low noise, flat gain, and small group-delay variation in the UWB frequency range. Simulation results shows a power gain of 12.5-dB, in a 7.6-GHz 3-dB bandwidth, a minimum noise figure of 3 dB, a reverse isolation better than 45 dB up to 10.6 GHz, and a record small group-delay variation of 12 ps. The LNA draws 6 mA from a 1.2-V power supply. [8]

Yeonsu Jang, Sungchan Kang, Young-Eil Kim, Jongryul Lee, Jae-Hoon Yi, and Kukjin Chun (2011) proposed a triple-band transceiver module for 2.3/2.5/3.5 GHz mobile WiMAX . It is fabricated in 0.13µm RF CMOS process with 3.5 dB NF of receiver and 1 dBm power of transmitter with 68-pin QFN package . The reduction in area of transceiver module by 9% is achieved by using embedded PCB. The transceiver module is tested by performing radio conformance test (RCT) and measuring carrier to interference plus noise ratio (CINR) and received signal strength indication (RSSI) in each 2.3/2.5/3.5 GHz frequency.[9]

Muhammad Khurram and S. M. Rezaul Hasan, (2012) proposed a design that takes the advantage of the current-reuse technique by "stacking" the active PMOS stage (that provides the inverting g_m-boosting gain between the source and the gate terminals of the input CG stage) on top of the input CG stage ("piggyback g_m-boosting"). The new proposed design reduced the power dissipation associated with the g_m-boosting, by implementing the "current-reused g_m-boosting", where the bias current is shared between the g_m-boosting CS stage and the amplifier CG stage. They represented a low-power CG UWB LNA architecture which implements a novel "current-reused-boosting" technique.

The topology also includes a front-end passive LC-band-pass filter for broadband input matching with sharp out-of-band roll-off. Proposed architecture represents a low-power CMOS transconductance "g_m" boosted CG UWB LNA, operating in the 3–5 GHz range, employing current-reuse technique. [10]

Saurabh Pargaien (2014) proposed a low power CMOS RF front-end LNA architecture, employing voltage controlled capacitor in input matching with inductive source degeneration topology and current reused technique. This LNA is designed for Bluetooth application that provide circuit performance at 2.4 GHz. The LNA schematic was simulated using TSMC 0.18 µm CMOS technology. From the simulation results, the fully integrated LNA exhibits a gain of 13.39 dB and a noise figure of 1.44 dB at 2.4 GHz, operated at a supply voltage of 1.5 V. The design process is simulated using Advance Design System (ADS).[11]

Jaehyuk Yoon and Changkun Park (2014) proposed a harmonic rejection technique using RC feedback for a differential CMOS amplifier. The third harmonic component of the drain node of the common-gate transistor is fed back to the drain of the common-source transistor to restrict the generation of the third harmonic component at the output of the LNA. The feedback of the fundamental component is minimized using the values of a resistor and a capacitor, which constitute the feedback loop. To verify the feasibility of the proposed technique for a linear amplifier, they designed a typical LNA and the proposed LNA in an identical process and with the same design parameters except for the feedback loop of the proposed LNA. The experimental results successfully demonstrate the feasibility of the proposed technique. [12]

Tran Van Hoi, Nguyen Xuan Truong, Bach Gia Duong (2015) proposed the design, simulation and fabrication of a two-stage LNA circuit with high gain and low noise figure using GaAs FET for frequency from 3.7 GHz to 4.2 GHz. It uses a two-stage cascade to create high gain and reduction in the noise figure. The Agilent' ADS 2009 package and machine LPKF Promomat C40 is used for the design, simulation and fabrication. A gain of 24.5dB with the operating frequency of 3.7 GHz to 4.2 GHz and noise figure of 1.1dB was obtained by the proposed LNA. [13]

Saurabh Pargaien, Abhishek Tomar and Ankur Bingh bist (2016) proposed a low power CMOS RF front-end LNA architecture, input matching with inductive degeneration source topology and current reused technique. This circuit provides performance from 3.34-3.92 GHz using a TSMC 0.18 µm CMOS process. The fully integrated LNA exhibits a gain of S_{11} is 17.74 dB, a noise figure less than 1dB from 1.4 GHz to 4.9 GHz, operating at a supply voltage of 1.8 V. The input insertion loss S_{11} is –23.26 dB and output loss S_{22} is -11.3 dB. [14]

CONCLUSION

In the published literature, several techniques have been reported to impart high performance LNA design for the 2–10 GHz UWB low-power applications. in these several techniques i.e. resistive termination, series shunt feedback, common gate connection and inductive degeneration have been used for the enhancement of the noise figure, gain and power dissipation. Current reuse technique is used to reduce power dissipation.

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